CLAIMS

1. An integrated circuit comprises one or more integrated circuit elements and one or more input/output pins, the one or more integrated circuit elements including an interface element for interfacing with external test circuitry, the interface element communicating with the external test circuitry via a single input/output pin dedicated for testing wherein the single pin connected operates with several logic thresholds and wherein the absence of positive action from the external test circuitry the integrated circuit defaults from test mode to normal mode.

2. An integrated circuit according to Claim 1 wherein the interface element is embedded into the integrated circuit as a single pin interface between the digital integrated circuit and the external test circuitry.

3. An integrated circuit according to Claim 2 wherein the interface element receives test data and commands from the external test circuitry in response to which a crash block controls and commands scan path elements within the digital integrated circuit and returns the resulting data to the external test circuitry.

4. An integrated circuit according to any preceding Claim wherein the logic thresholds define several logic levels which enable data and timing signals to be differentiated on a single pin.

5. An integrated circuit according to any preceding Claim wherein a "pad detection" detector determines whether there is a connection an external tester or other external circuitry by assessing the voltage on the single pin.

6. An integrated circuit according to any preceding claim wherein if a voltage on the single pin is held at a voltage below "low" for a period of time determined by an "escape 0 timer" then the integrated circuit will decide there is no tester connected to the single pin.